WHAT IS CLAIMED IS:

1. A processing system for an imager device comprising:

a camera system for producing an imager signal, said camera system including a shutter settable for shutter gain;

a correlated double sample circuit for receiving data from an imager;

said correlated double sample circuit being adapted for variable gain amplification;

an analog-to-digital converter (ADC) coupled to said CDS circuit;

a digital gain circuit (DGC) coupled to said correlated double sample circuit; and

an automatic gain control (AGC) circuit coupled to said DGC, said correlated double sample circuit, and said shutter; effective for exercising distributed gain control.

2. A processing system according to claim 1, including a timing circuit for controlling shutter gain.

3. A distributed gain control circuit (DGCC) comprising:

an imager signal source including a shutter;

a timing circuit for controlling said shutter and the production of signals from said imager signal source;

a CDS/VGA system for receiving imager signals from said imager signal source;

an analog to digital converter connected to said CDS/VGA system for receiving an amplified imager signal stream from said CDS/VGA system and converting the amplified imager signal stream into digital form;

a digital gain circuit connected to said analog to digital converter; and

an automatic gain control (AGC) circuit for receiving an output digital level from said digital gain circuit for controlling the gain of said CDS/VGA system, said digital and shutter gain circuit.

4. The DGCC according to claim 3 wherein said AGC circuit is coupled to said timing circuit for controlling the production of signals from said imager signal source.

5. A method of gain control in an imaging system having a shutter, a digital gain circuit, and a CDS/VGA circuit, including:

determining total gain for an imaging system;

determining the level of shutter gain to be applied in the operation of the imaging system;

determining the level of analog gain to be applied in the operation of the imaging system; and

determining the level of digital gain to be applied in the operation of the imaging system.

6. The method according to claim 5 wherein each gain setting for said imaging system is applied for the duration of a single frame.

7. The method according to claim 5 including hierarchically adjusting shutter gain, analog (VGA) gain, and digital gain.

8. The method according to claim 7 wherein the shutter gain has maximum and minimum shutter gain values.

9. The method according to claim 7 wherein the analog (VGA) gain has maximum and minimum analog gain values.

10. The method according to claim 7 wherein the chip gain has a maximum and a minimum gain value.

11. The method according to claim 7 wherein the digital gain has a maximum and a minimum value.

12. The method according to claim 8 wherein the analog (VGA) gain and the digital gain remain at a constant level as the shutter gain is varied.

13. The method according to claim 8 wherein the shutter gain and the analog (VGA) gain remain at a constant level as the digital gain is varied.

14. The method according to claim 8 wherein the shutter gain and the digital gain remain at a constant level as the analog (VGA) gain is varied.

15. The method according to claim 12 or 13 or 14, wherein said constant level is user-settable.

16. A method of setting a minimum gain level to ensure AGC operation at selected CCD saturation levels by preventing the CCD from saturating under bright conditions.

17. A method of AGC operation including:

setting a selected programmable maximum combined gain level;

setting a selected programmable maximum shutter gain level;

setting a selected minimum gain level; and

individually adjusting shutter gain, analog (VGA) gain and digital gain in substantially comparable gain steps.

18. The method of AGC operation according to claim 17 wherein shutter gain has predetermined gain steps.

19. The method of AGC operation according to claim 17 wherein analog (VGA) gain has predetermined gain steps.

20. The method of AGC operation according to claim 17 wherein digital gain has predetermined gain steps.

21. The method of AGC operation according to claim 17 wherein shutter gain, analog (VGA) gain and digital gain, each have predetermined gain step sizes.

22. The method of AGC operation according to claim 17 wherein the gain step sizes for shutter gain, analog (VGA) gain, and digital gain are substantially the same.

23. The method of AGC operation according to claim 17 whereby gain changes due to modification of shutter gain, analog (VGA) gain, and digital gain are not user-discernible.

24. The method of AGC operation according to claim 17 wherein AGC gain changes below the selected programmable maximum shutter gain level are implemented exclusively with shutter gain changes.

25. The method of AGC operation according to claim 17 wherein AGC gain changes in excess of maximum shutter gain are implemented exclusively as chip gain changes.

26. The method of AGC operation according to claim 17 wherein chip gain changes above maximum VGA gain are implemented exclusively as digital gain.

27. The method of AGC operation according to claim 17 wherein chip gain changes below the maximum VGA gain are implemented exclusively as analog or VGA gain.

28. The method of AGC operation according to claim 17 wherein incremental gain changes within the combined gain range are programmable with respect to maximum total gain, minimum chip gain, and maximum shutter gain and are substantially constant, seamless, and continuous.

29. A method of gain control including:

sampling input images at an ambient light source set to a predetermined frequency; and

cancelling a selected shutter gain change with an equal but opposite analog gain change for a predetermined gain range.

30. The method of gain control according to claim 29 including producing an extended flickerless gain range of 6 dB.

31. The method of gain control according to claim 29 including employing a hysteresis loop to prevent oscillation between one and two cycle gain levels.

32. A gain control system for splitting an input gain code value into prioritized gain components, including:

a first gain splitter subsystem (FSS) for receiving an input gain code value and producing shutter gain code and chip gain code values; and

a second splitter subsystem (SSS) connected to said first splitter subsystem, for receiving a chip gain code value from the first splitter subsystem;

said second splitter subsystem configured for producing a digital gain value and an analog (VGA) gain value from a received chip gain value.

33. The gain control system according to claim 28 wherein said FSS is configured to produce no more than a selected minimum chip gain code value until a settable maximum shutter gain code value is reached.

34. The gain control system according to claim 28 wherein said FSS and SSS are configured to produce a continuous total gain code which is the sum of shutter, analog, and digital gain codes produced by said FSS and SSS.